A DESIGN METHOD FOR HIGH EFFICIENCY CLASS F HBT AMPLIFIERS

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ABSTRACT

In this paper, we report on the Class F operation of HBTs. A temperature dependent model of a 240μm^2 GaInP/GaAs HBT (THOMSON-CSF) was extracted from pulsed I/V and pulsed S parameter measurements and validated by load-pull measurements. An extensive large signal HB analysis, based on "the substitute generator technique", was achieved to optimize the load impedance at harmonic frequencies required for class F operation.

Furthermore, the performances of the transistor in terms of added power, power added efficiency and dissipated power, were investigated under different bias modes (ie: constant base voltage, constant base current and self bias modes). We will show that the bias mode has a great influence on the HBT linearity.

I INTRODUCTION

HBTs have emerged as valuable devices for microwave power amplification. There are now considered as concurrents to MESFETs for the design of the next generation of solid state amplifiers.

High efficiency class B and C HBT amplifiers have been already reported [1],[2]. However, the class F operation of HBTs has never been demonstrated. We demonstrate in this paper that high efficiency class F operating mode is possible if the dynamic load-line of the transistor goes into the very low collector-emitter voltage region (saturated region) where the collector current strongly depends on both collector-base and base-emitter voltages.

Under such conditions, a square collector-voltage waveform can be obtained if harmonics are appropriately loaded.

Such an operating mode is also well suited for high efficiency operation at low collector-voltage ($Vce_0 \pi 3V$). It is therefore expected to be used for L. Band personal communication systems.

II BASIC CONSIDERATIONS ON HBT I/V CHARACTERISTICS

The basic electrical characteristic of HBTs is the exponential dependence of the collector current on the base-emitter voltage (equation 1).

$$(1)\quad ic(t) = Is.\left[e^{(\alpha.Vbe(t))} - 1\right]$$

Let us consider a sinusoidal emitter voltage:

$$Vbe(t)=Vbe_0+Vbe_1.\cos(\omega t)$$

The collector current can be expressed in terms of a Bessel serie expansion:

$$(2)\quad ic(t) = i_0 + \sum_{n=1}^{\infty} 2I_n(x)\cos(n.\omega t)$$

where x is αVbe_1 and In(x) are the modified Bessel functions.

As In(x) are positive values, the first and the third harmonic components of the collector current are always in phase.

If the collector current (equation 2) flows in a passive network, it cannot produce a square voltage waveform required for class F operation, simply because the first and the third harmonics of a square wave are in opposite phase [3], [4].

$$(3)\quad Vce(t)_{square}=Vce_0-Vce_1.\cos(\omega t)+Vce_3.\cos(3\omega t)$$

with Vce_3 close to $Vce_1/6$

In conclusion, the class F operation cannot be performed if the HBT collector current source is only controlled by the base-emitter voltage.

Nevertheless, we demonstrate in this paper that class F operation is possible at low collector-emitter voltages (saturated region) where the emitter current depends on both collector-emitter and collector-base voltages.

III TEMPERATURE DEPENDENT LARGE SIGNAL MODEL

We used for the study reported in this paper a 240μm^2 four emitter finger HBT (THOMSON foundry) [5]. The equivalent circuit of this transistor is given in figure 1 [6]. A non linear model was extracted from pulsed I/V and pulsed S parameter measurements [7]. The model takes into account the temperature dependence of the convective non linear elements (diodes and collector current source). The simulated DC characteristics are shown in figure 2.

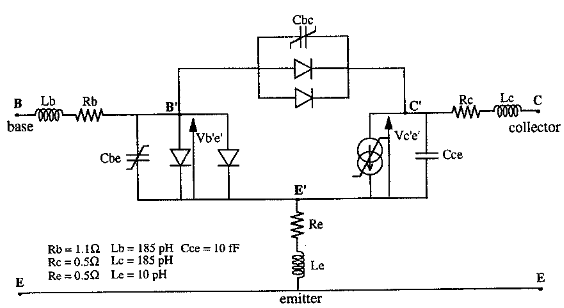

Figure 1: HBT non linear model

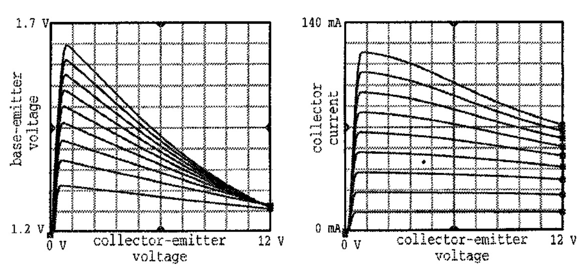

Figure 2: Simulated DC characteristics

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Load-pull measurements were performed at 1.8 GHz to validate the HBT large signal model. The bias conditions of the transistor were (Vbe_0=1,0V ; Vce_0=7,0V). The load impedance at the fundamentaloperating frequency was optimized for maximum added power while the load impedance at the signal harmonics was 50Ω. The variations of added power and power added efficiency versus input power (measurements and simulated data) are given in figure 3.

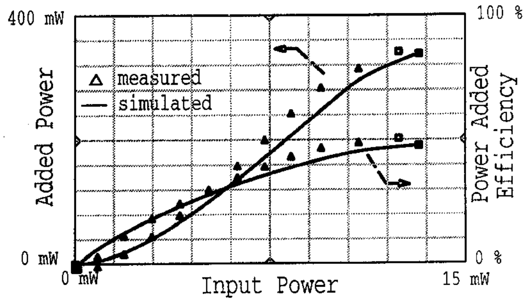


Figure 3: Measured and simulated added power and power added efficiency (50Ω)

IV LARGE SIGNAL HB ANALYSIS

The large signal analysis of any transistor and the optimisation of high efficiency operating classes can be performed in a very straightforward way using the "Substitute Generator Technique". This method which can be easily implemented in commercially available softwares, consists on forcing voltage waveforms at both accesses of transistors with independant generators (figure 4).

A sinusoidal input signal ($Vbe(t)=Vbe_0+Vbe_1.\cos(\omega t)$) is imposed for the simulation of high efficiency classes B, C, and F. Note that other input waveforms (e.g.: square voltages) can be used for the study of classes E or D.

The collector-emitter voltage Vce(t) is forced to:

$$Vce(t)=Vce_0+Vce_1.\cos(\omega_0.t+\theta_1)+Vce_2.\cos 2.\omega_0.t+\theta_2)+Vce_3.\cos(3.\omega_0.t+\theta_3) \quad (4)$$

(three harmonic components are generally sufficient).

-For the analysis of classes B and C, we will impose:

$$Vce(t)=Vce_0-Vce_1.\cos(\omega_0.t+\theta_1)$$

-For the analysis of class F, we will impose:

$$Vce(t)=Vce_0.(1-k_1.\cos(\omega_0.t+\theta_1)+k_3.\cos(3.\omega_0.t+\theta_3))$$

$.k_1$ is in the order of 1.15, k_3 is in the order of 0.2 and θ_1. θ_3 need to be adjusted so as to obtain a square voltage waveform across the HBT intrinsic collector current source.

Once an HB analysis is completed, the collector current given by the output probe is:

$$ic(t) = Ic_0 + \sum_{n=1} 2Ic_n(x)\cos(n.\omega t + \varphi_n)$$

At every harmonics, the following relationship must be verified:

$$\mathrm{Re}\left(\frac{-Vce_n.e^{j\theta n}}{Ic_n.e^{i\varphi n}}\right) = \mathrm{Re}(ZL_n) > 0 \quad \text{(Re denotes real part).}$$

That means that ZL_n which is the load impedance at the n^{th} signal harmonic must be passive.

Following the method described hereabove,simulations of classes B and F were performed. In both cases, the transistor was biased at (Vbe_0=1,0V ; Vce_0=7,0V). Optimized current/voltage waveforms and dynamic load-lines for maximum added power are shown in figure 5. **It is observed that class F is possible if the load-line goes into the saturated region.**

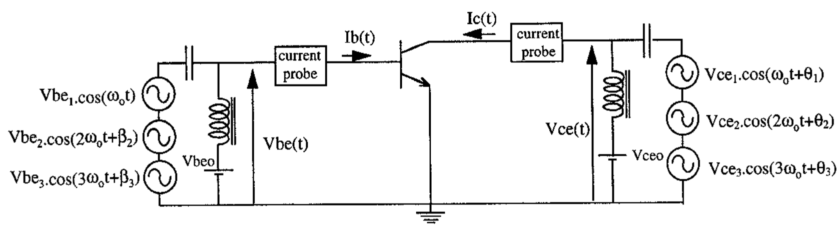


Figure 4: Substituate generator technique

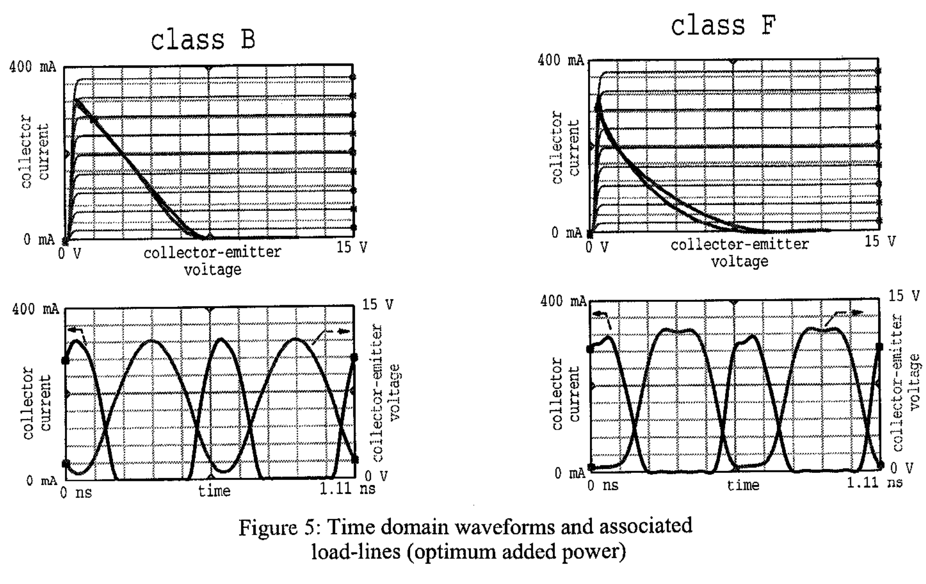
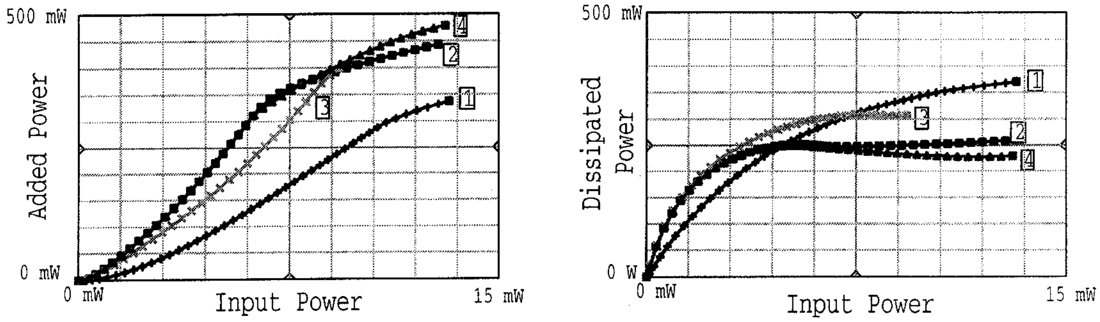
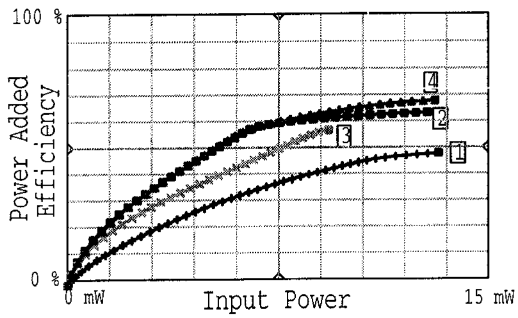


Figure 5: Time domain waveforms and associated load-lines (optimum added power)





case	ZL(fo)	ZL(2fo)	ZL(3fo)	
1	(33+j4) Ω	50Ω	50Ω	
2	(38+j6) Ω	short	50Ω	
3	(32+j3) Ω	short	short	class B
4	(39+j6) Ω	short	(6+j66) Ω	class F

Figure 6: Power characteristics for different harmonic terminations

Study on harmonic terminations and DC bias modes:

The variations of added power, power added efficiency and dissipated power versus RF input power were studied under constant base voltage bias conditions . Results obtained at 1.8GHz for different harmonic terminations are illustrated in figure 6. The HBT exhibits 57% P.A.E. and 400mW added power when operated in class B while it exhibits 68% P.A.E and 480mW added power when operated in class F.

It is clearly observed that **class F is attractive to optimize P.A.E. and to minimize the power dissipated by the transistor under large signal operation**. The best operating class (class F) was validated by harmonic load-pull measurements [8]. A comparaison between measurements and simulated results is shown in figure 7.

Under large signal class F operation, the DC base current is equal to 7mA. It is of great interest to study the behavior of the transistor under a constant DC base current of 7mA [9]. For that, the HBT is biased with a DC current source (figure 8), the load impedance at the signal harmonics is the one that has been previously optimized, and the input RF power level is swept. Under constant base current bias mode, **the operating class of the transistor moves from class A (at low level) to class B (medium RF level) and class F (large signal conditions)**. The variations of added power, power added efficiency and dissipated power versus RF input power corresponding to the three bias modes sketched in figure 8 are illustrated in figure 9. Trade-offs between power gain, added power and linearity can be obtained under self bias conditions.

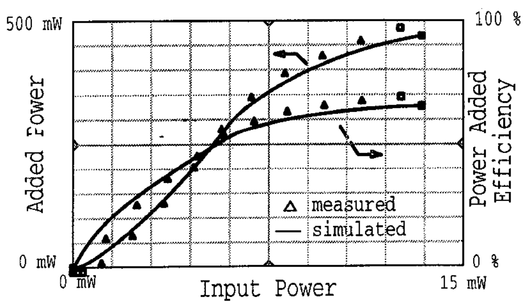


Figure 7: Measured and simulated power characteristics (class F)

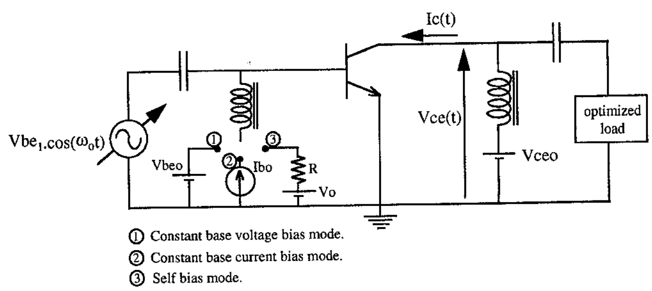
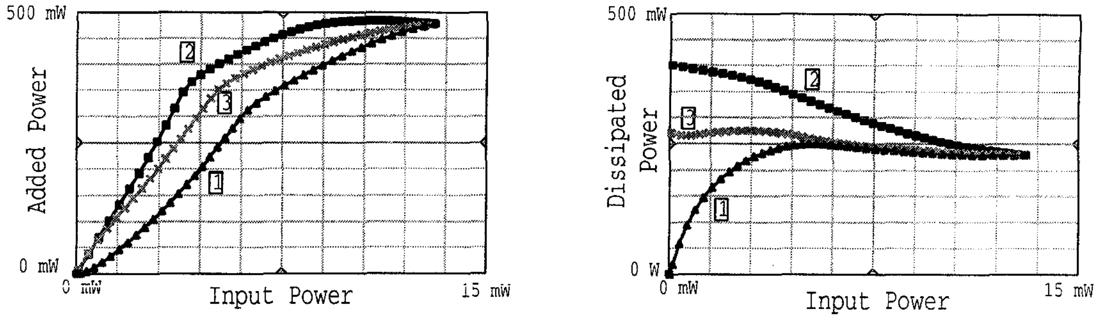
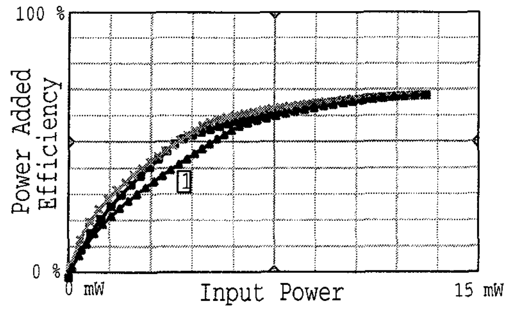


Figure 8: Biasing modes of HBT





case	bias condition
1	constant base voltage
2	constant base current
3	self bias condition

Figure 9: Power characteristics under different biasing modes

CONCLUSION

Class F operation of HBTs has been demonstrated in this paper. The influence of the load impedance at the signal harmonics on added power, power added efficiency and dissipated power has been shown. As HBTs potentialities are more limited by thermal aspects than by electrical ones, class F operation mode reveals to be very attractive because it allows to minimize dissipated power.

Following the method described in this article, high efficiency amplifiers operating at low collector bias voltages ($Vce_0 \leq 3V$) can be designed. One of the main use of such amplifiers is expected to be in personal communication systems.

It has to be noticed that high efficiency operation at low collector voltage requires very large HBTs in order to have a large collector current swing so that a significant output power can be reached. Results obtained with larger HBTs will be given in the final paper.

The variations of output power, P.A.E., and dissipated power versus input power under constant base current bias conditions have also been shown and discussed in this article.

Trade-offs between P.A.E. and linearity of HBTs can be obtained under suitable biasing conditions.

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